forming a source region, a drain region and a channel region formed between the source and drain regions,

wherein the two p-channel thin film transistors are connected in series,

wherein an off current from each of the p-channel thin film transistors is less than 10^{-12} A where a voltage of the drain region is 1V, and

wherein a pixel electrode is connected to a data line without any n-channel thin film transistor connected therebetween.

9. (Twice Amended) A method of manufacturing a display device, said display device comprising:

a pixel portion and a driving circuit portion;

at least two p-channel thin film transistors being formed in the pixel portion;

each of the two p-channel thin film transistors fabricated through the method comprising:

forming a semiconductor island over a substrate;

forming a gate electrode adjacent to the semiconductor island with a gate insulating film therebetween;

forming a source region, a drain region and a channel region formed between the source and drain regions,

wherein the two p-channel thin film transistors are connected in series,

wherein an off current from each of the p-channel thin film transistors is less than 10^{-12} A where a voltage of the drain region is 1V, and

wherein a pixel electrode is connected to a data line without any n-channel thin film transistor connected therebetween.

15. (Twice Amended) A method of manufacturing a semiconductor device, said semiconductor device comprising:

at least a first p-channel thin film transistor and a second p-channel thin film transistor in a pixel portion;

a transmission gate including a CMOS circuit, said CMOS circuit including at least an n-channel thin film transistor and a third p-channel thin film transistor;

each of the first, second and third p-channel thin film transistors fabricated through the method comprising:

forming a semiconductor island over a substrate;

forming a gate electrode adjacent to the semiconductor island with a gate insulating film therebetween;

forming a source region, a drain region and a channel region formed between the source and drain regions,

wherein the first and second p-channel thin film transistors are connected in series,

wherein an off current from each of the first, second and third p-channel thin film transistors is less than 10^{-12} A where a voltage of the drain region is 1V, and

wherein a pixel electrode is connected to a data line without any n-channel thin film transistor connected therebetween.